Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

**PAD FUNCTIONS:**

1. **ADJUST**
2. **VOUT**
3. **VOUT**
4. **V IN**

**.065”**

**.040”**

**3**

**1**

**MASK**

**REF**

**3**

**1**

**7**

**L**

**C**

**4**

**2**

**Top Material: Al**

**Backside Material: Si**

**Bond Pad Size: .004” X .004”**

**Backside Potential:**

**Mask Ref: 317L C**

**APPROVED BY: DK DIE SIZE .040” X .065” DATE: 2/4/21**

**MFG: NATIONAL SEMI THICKNESS .011” P/N: LM317L**

**DG 10.1.2**

#### Rev B, 7/1